REMARKS

This Amendment seeks to place this application in condition for allowance. Several of the pending claims have been amended. No new matter has been added.

INFORMATION DISCLOSURE STATEMENT

In compliance with the duty of disclosure set forth in 37 C.F.R. §1.56, an Information Disclosure Statement ("IDS") is being mailed concurrently herewith. A copy of the IDS and modified Form PTO-1449 is included herewith.

It should be noted that three (3) of the documents listed in the PTO-1449 have been brought to the Applicants' attention by way of the plaintiff in a proceeding pending in U.S. District Court for the District of Delaware, namely in Micron Technology Inc. v. Rambus Inc. The plaintiff identified the documents as prior art against the inventions claimed in, among others, U.S. Patent 6,034,918. The '918 patent is a grandparent of the instant Application.

CONCLUSION

Applicants request entry of the foregoing amendment. Applicants submit that all of the claims present patentable subject matter. Accordingly, Applicants respectfully request allowance of all of the claims.

Respectfully submitted,

Date: August 8, 2001

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EXHIBIT A

VERSION WITH MARKINGS TO SHOW CHANGES MADE

151. (Twice Amended) A method of operation of a synchronous memory device, wherein the memory device includes an array of memory cells, the method of operation comprises:

receiving an external clock signal;

receiving block size information, wherein the block size information defines an amount of data to be output by the memory device in response to a first operation code;

sampling [receiving] the first operation code synchronously with respect to the external clock signal wherein the first operation code instructs the memory device to perform a read operation; and

outputting the amount of data in response to the first operation code.

152. (Twice Amended) The method of claim 151 wherein the block size information also defines an amount of data to be input by the memory device, wherein the amount of data is input in response to a second operation code, and wherein the second operation code instructs the memory device to perform a write operation, the method further including:

sampling [receiving] the second operation code synchronously with respect to a transition of the external clock signal; and

inputting the amount of data in response to the second operation code.

156. (Twice Amended) The method of claim 151 wherein the memory device samples [receives] the block size information synchronously with respect to the external clock signal.

161. (Twice Amended) The method of claim 151 wherein the block size information is an encoded value and wherein the block size information is sampled synchronously with respect to a rising or falling edge of[_] the external clock signal.

165. (Twice Amended) A method of controlling a synchronous memory device by a controller, wherein the memory device includes an array of memory cells, the method of controlling the memory device comprises:

issuing [providing] block size information to the memory device synchronously with respect to an external clock signal, wherein the block size information defines an amount of data to be output by the memory device; and

issuing a first operation code to the memory device synchronously with respect to the external clock signal, wherein the first operation code instructs the memory device to perform a read operation.

176. (Twice Amended) A synchronous dynamic random access memory device having at least one memory section including a plurality of memory cells, the memory device comprising:

clock receiver circuitry to receive an external clock signal;

input receiver circuitry, including a first plurality of input receivers to sample [receive] block size information synchronously with respect to the external clock signal, wherein the block size

information defines an amount of data to be output by the memory device in response to a first operation code; and

a plurality of output drivers to output the amount of data in response to the first operation code.

179. (Twice Amended) The memory device of claim 176 wherein the input receiver circuitry [receives] samples the first operation code synchronously with respect to the external clock signal.